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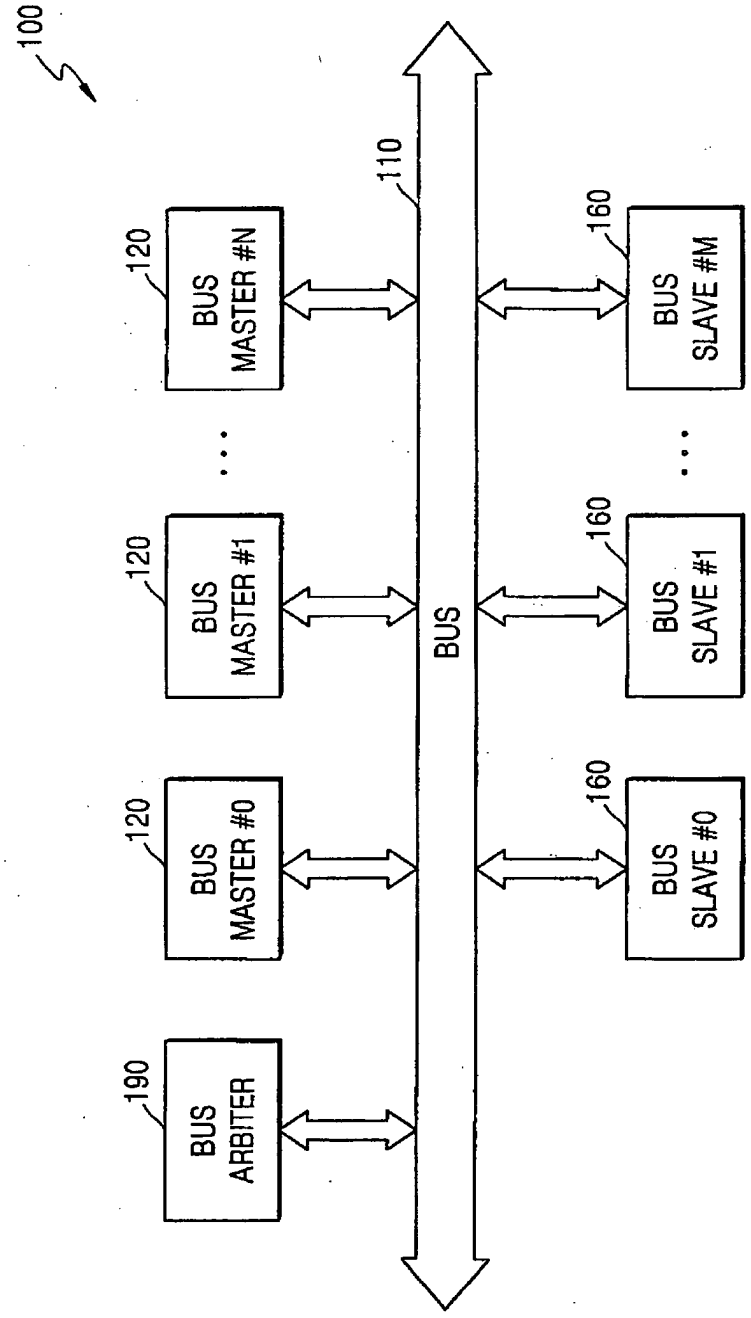
SYSTEM ON A CHIP HAVING A SYSTEM BUS, AN EXTERNAL BUS, AND A BUS ARBITER WITH PROGRAMMABLE PRIORITIES FOR BOTH BUSES, SOFTWARE, AND METHOD FOR ASSIGNING PROGRAMMABLE PRIORITIES

Attorney Docket No. 9898-172/Application No. 09/773,874

FIG. 1 (PRIOR ART)



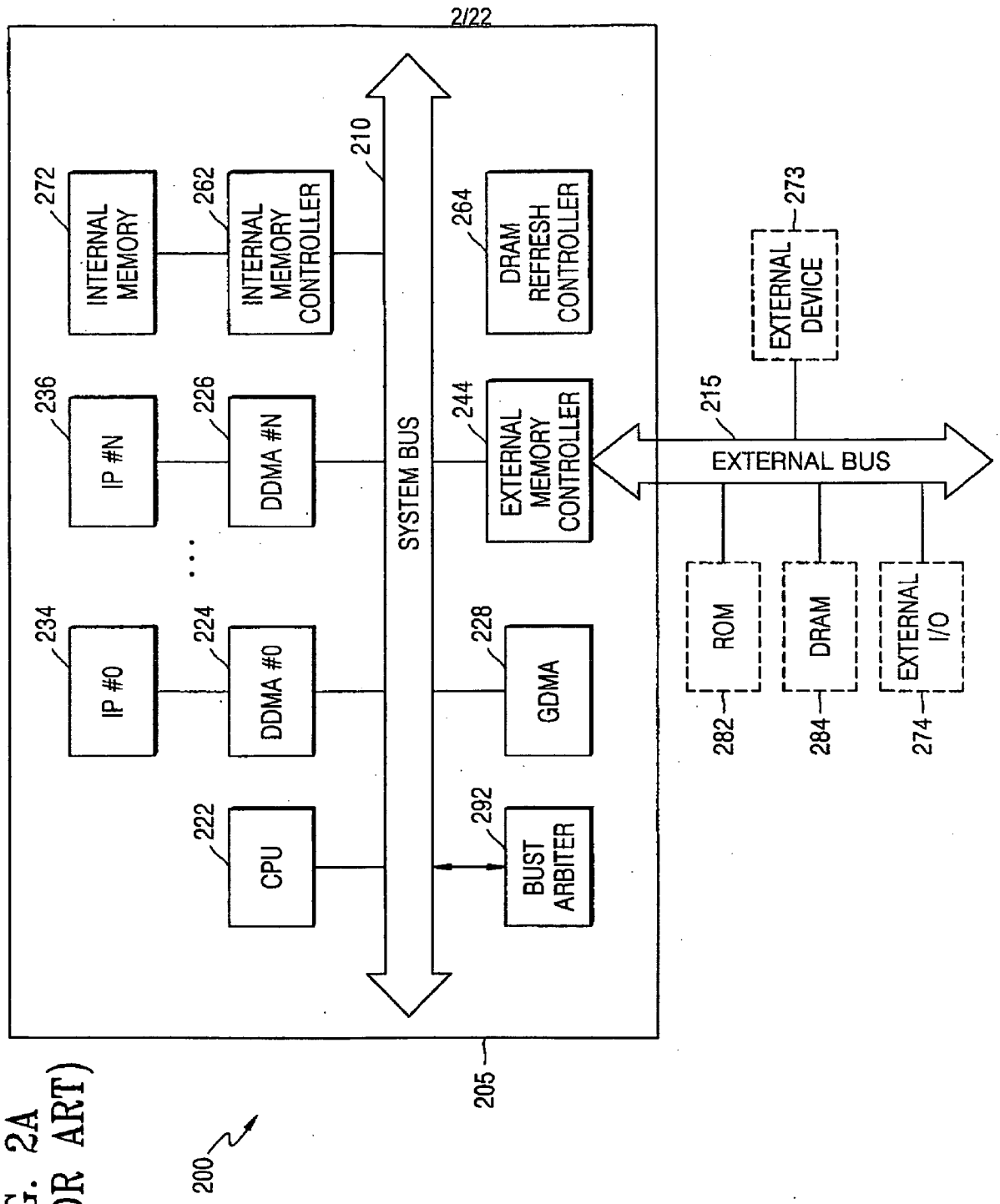
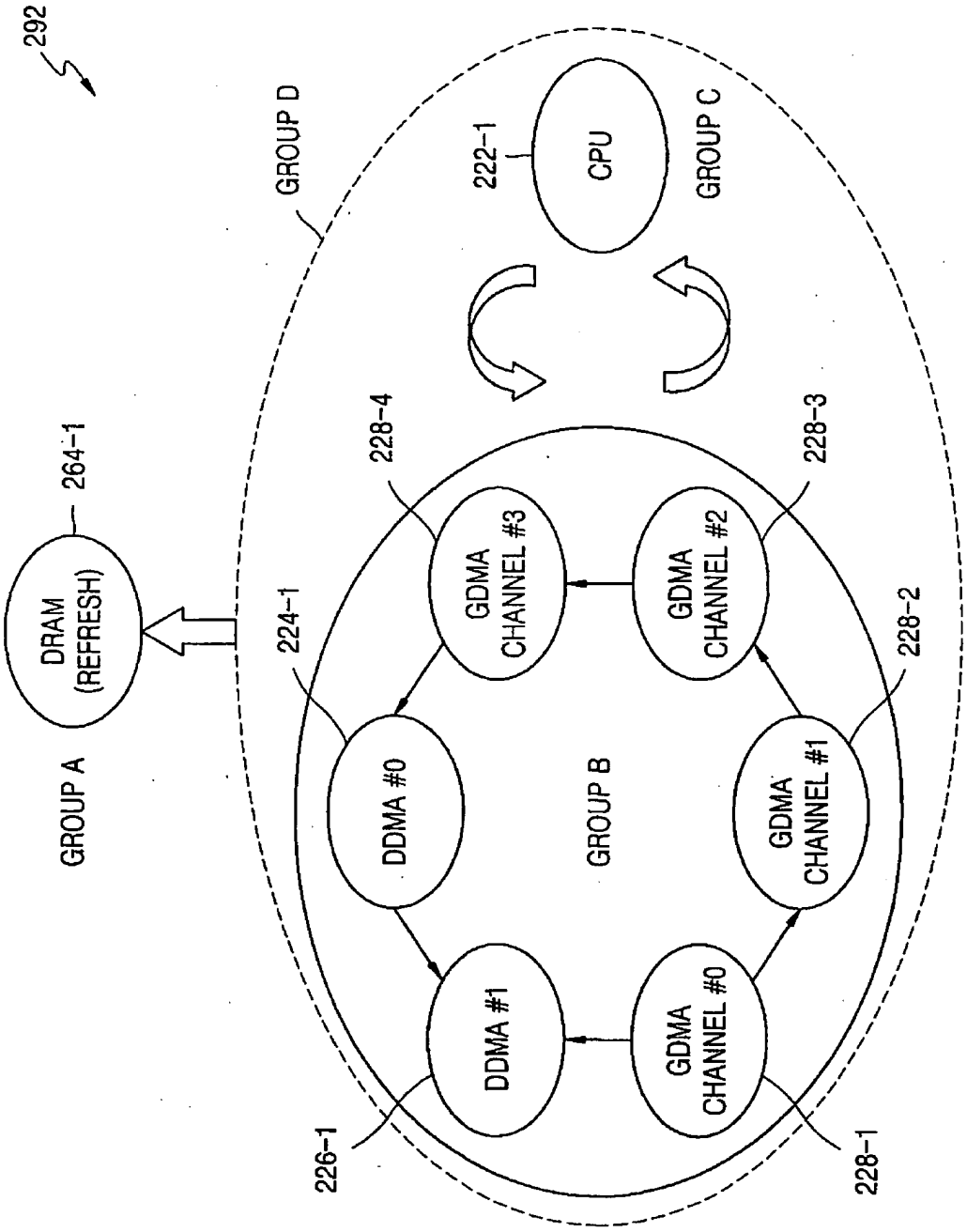


FIG. 2A
(PRIOR ART)

FIG. 2B (PRIOR ART)



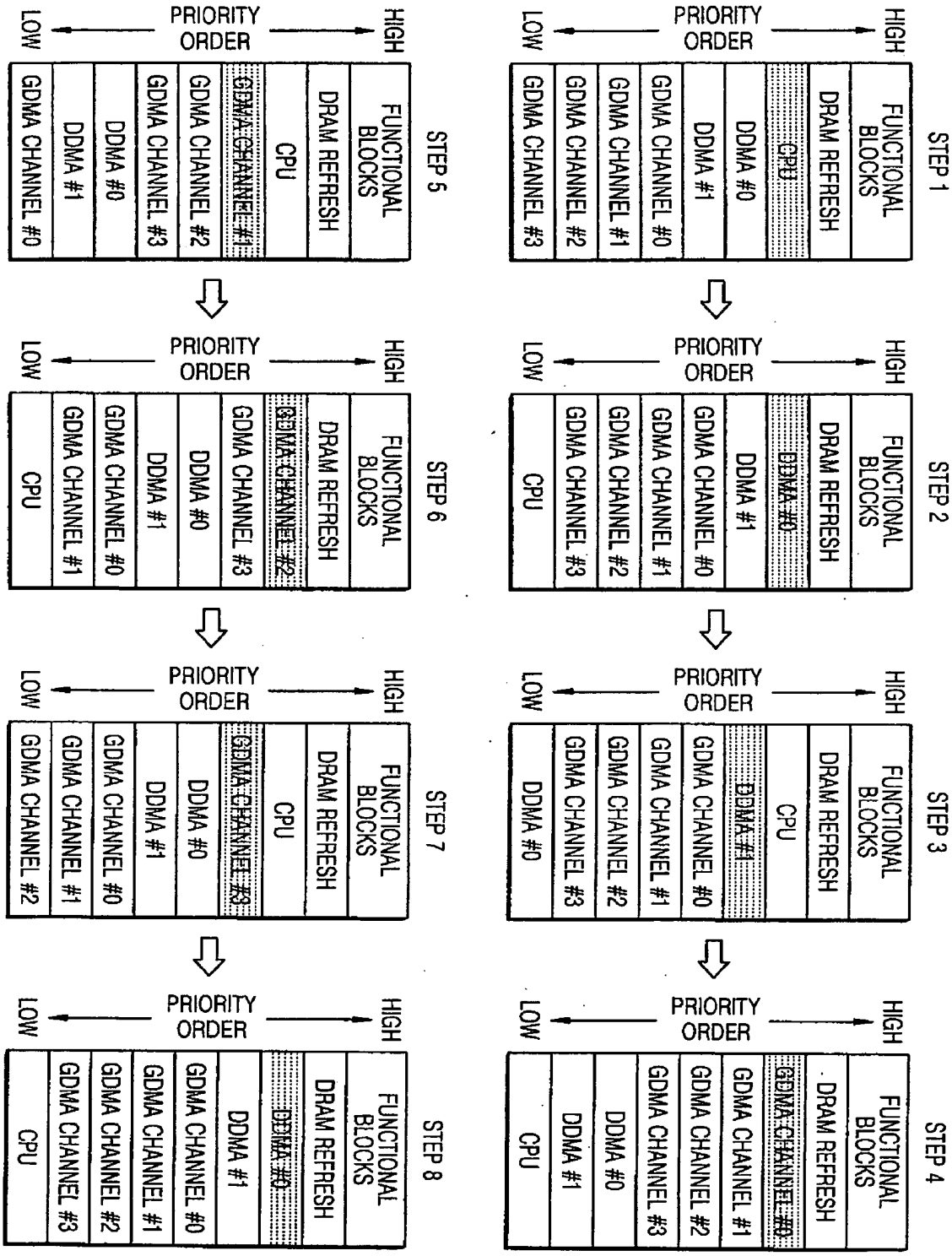


FIG. 2C (PRIOR ART)

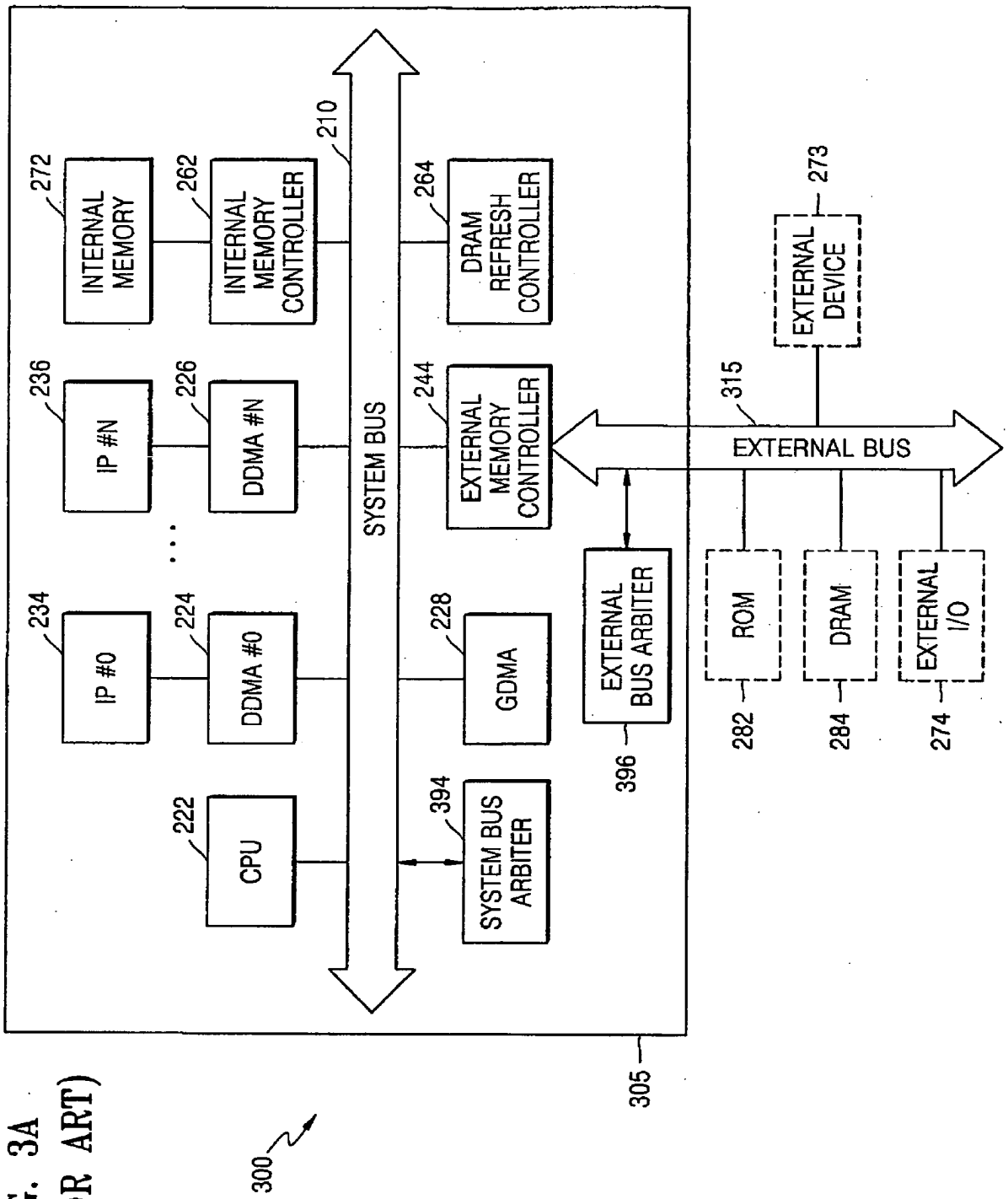


FIG. 3A
(PRIOR ART)

FIG. 3B (PRIOR ART)

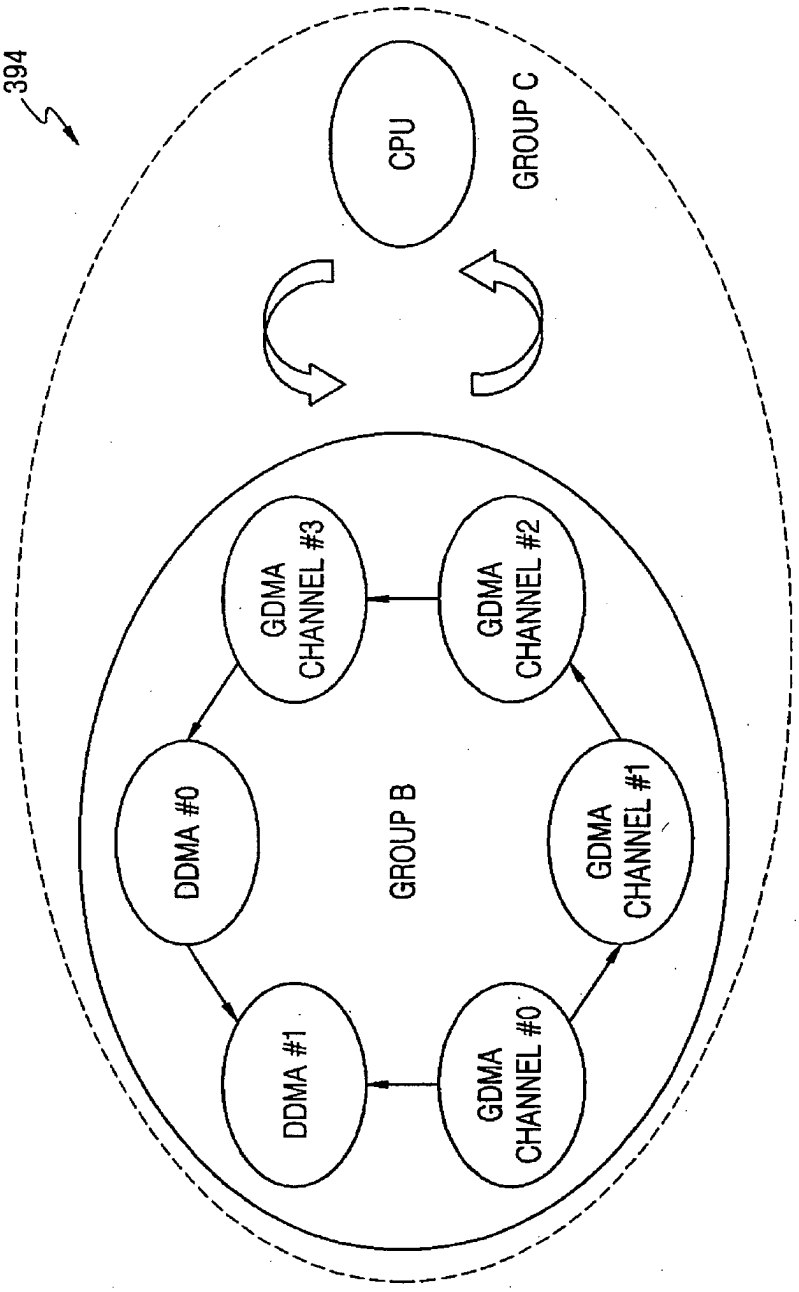
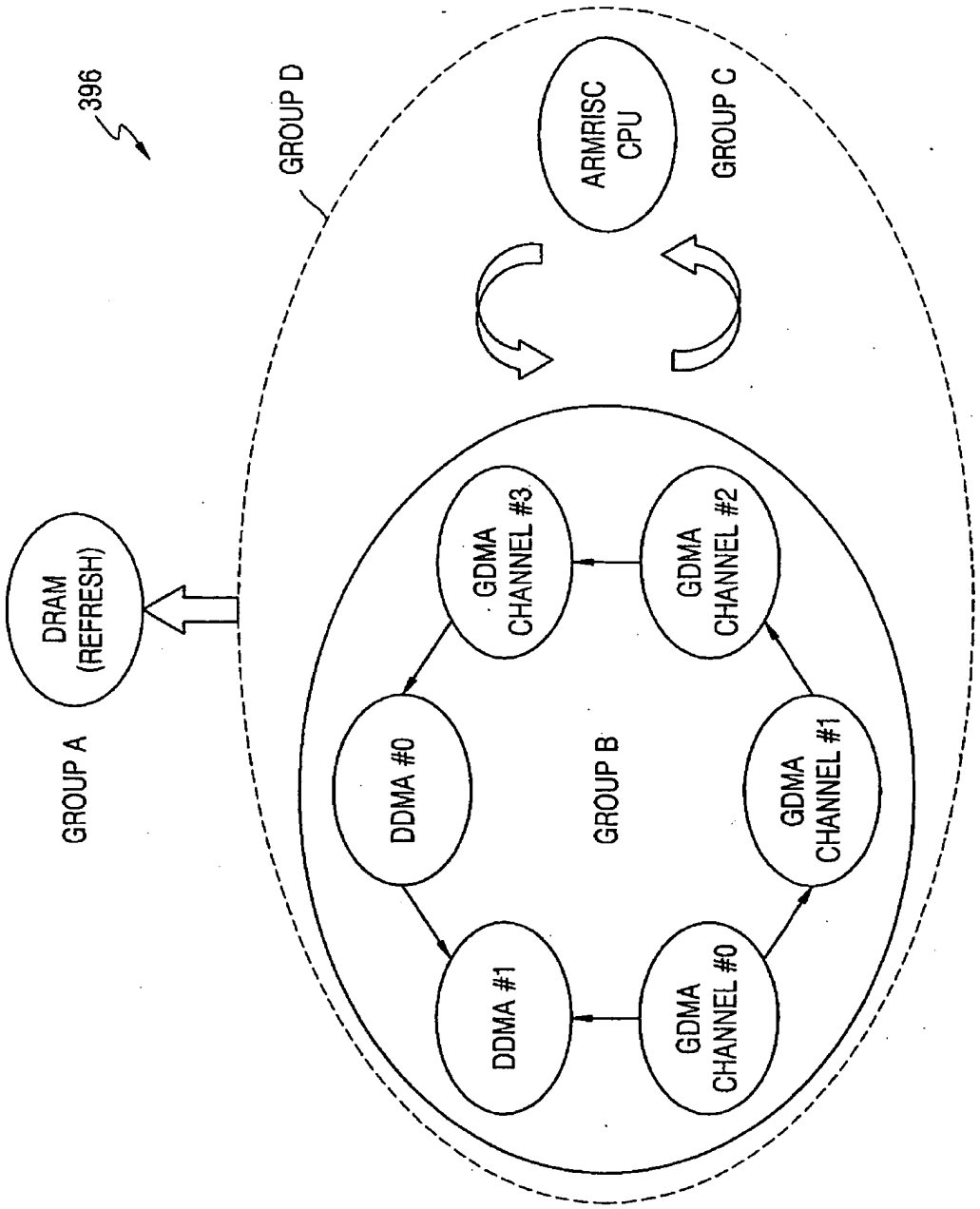


FIG. 3C (PRIOR ART)



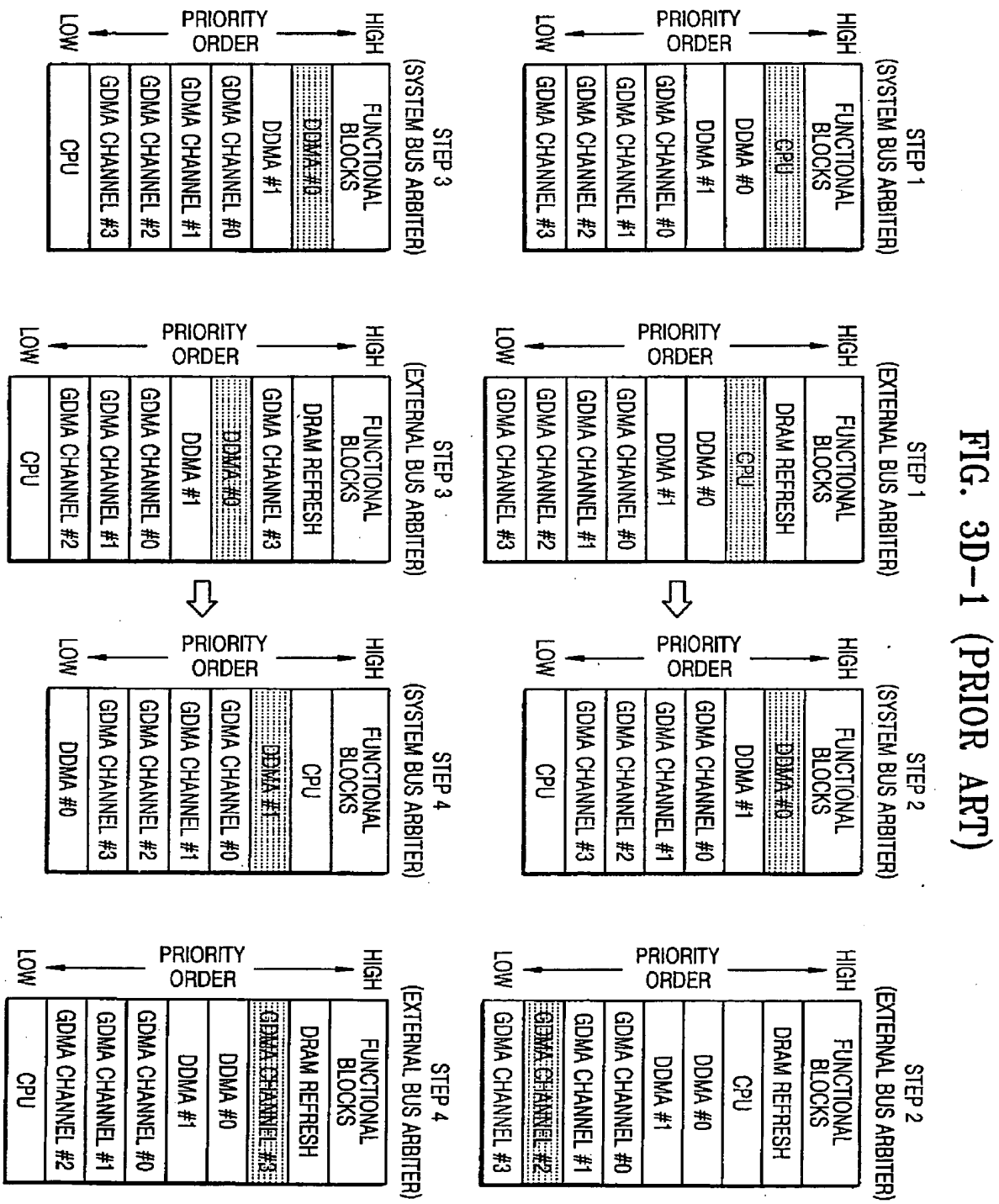


FIG. 3D-1 (PRIOR ART)

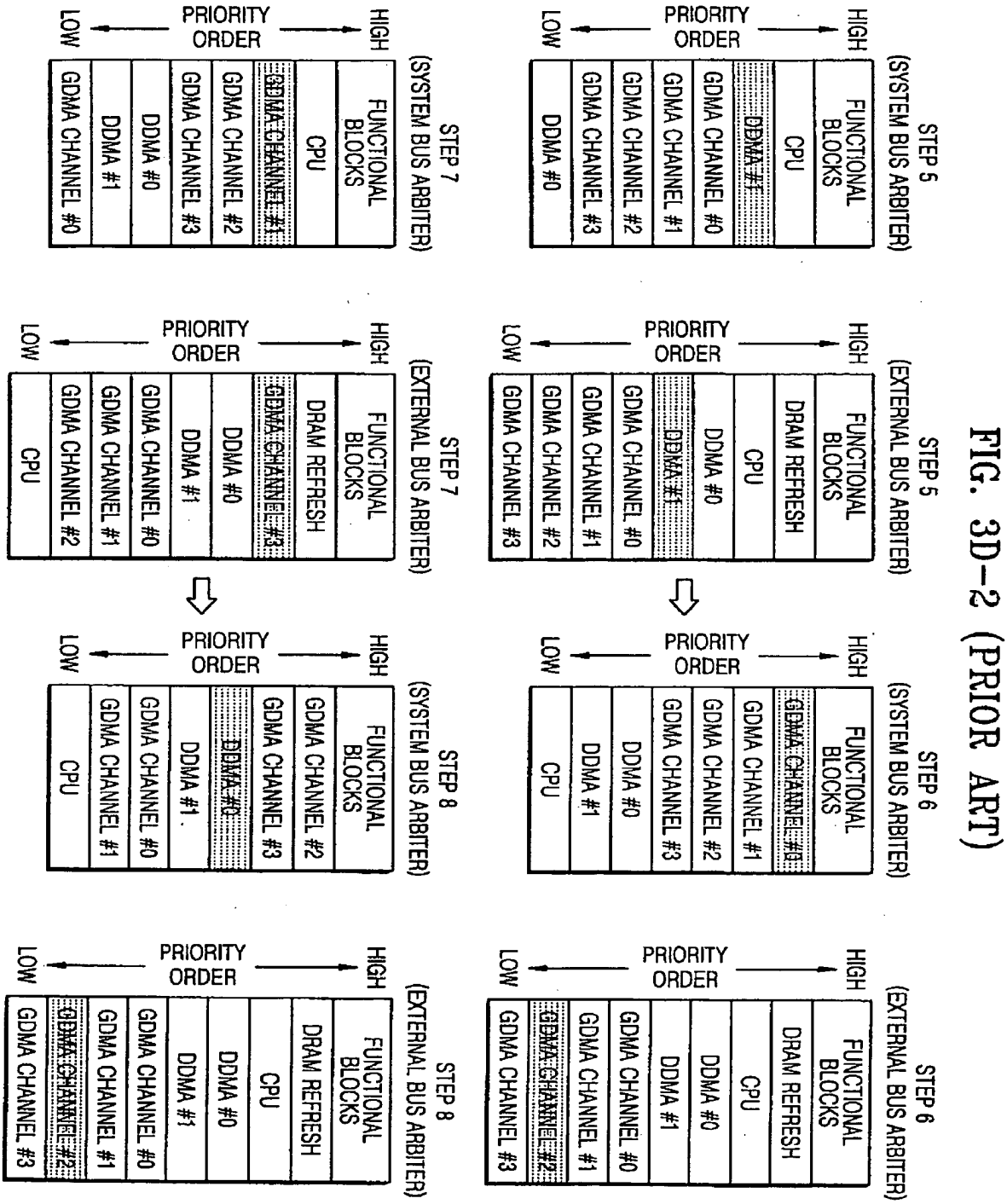


FIG. 3D-2 (PRIOR ART)

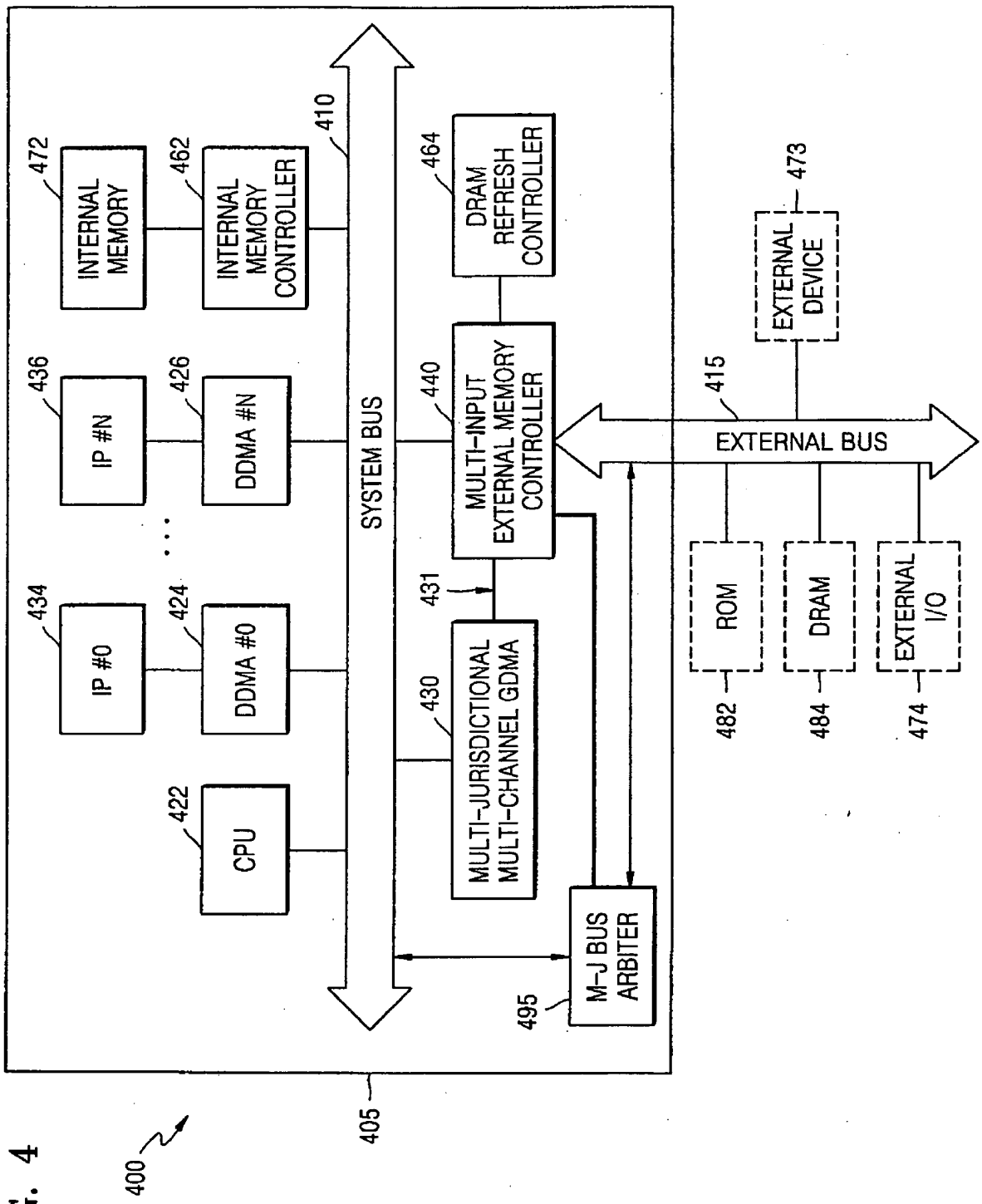


FIG. 4

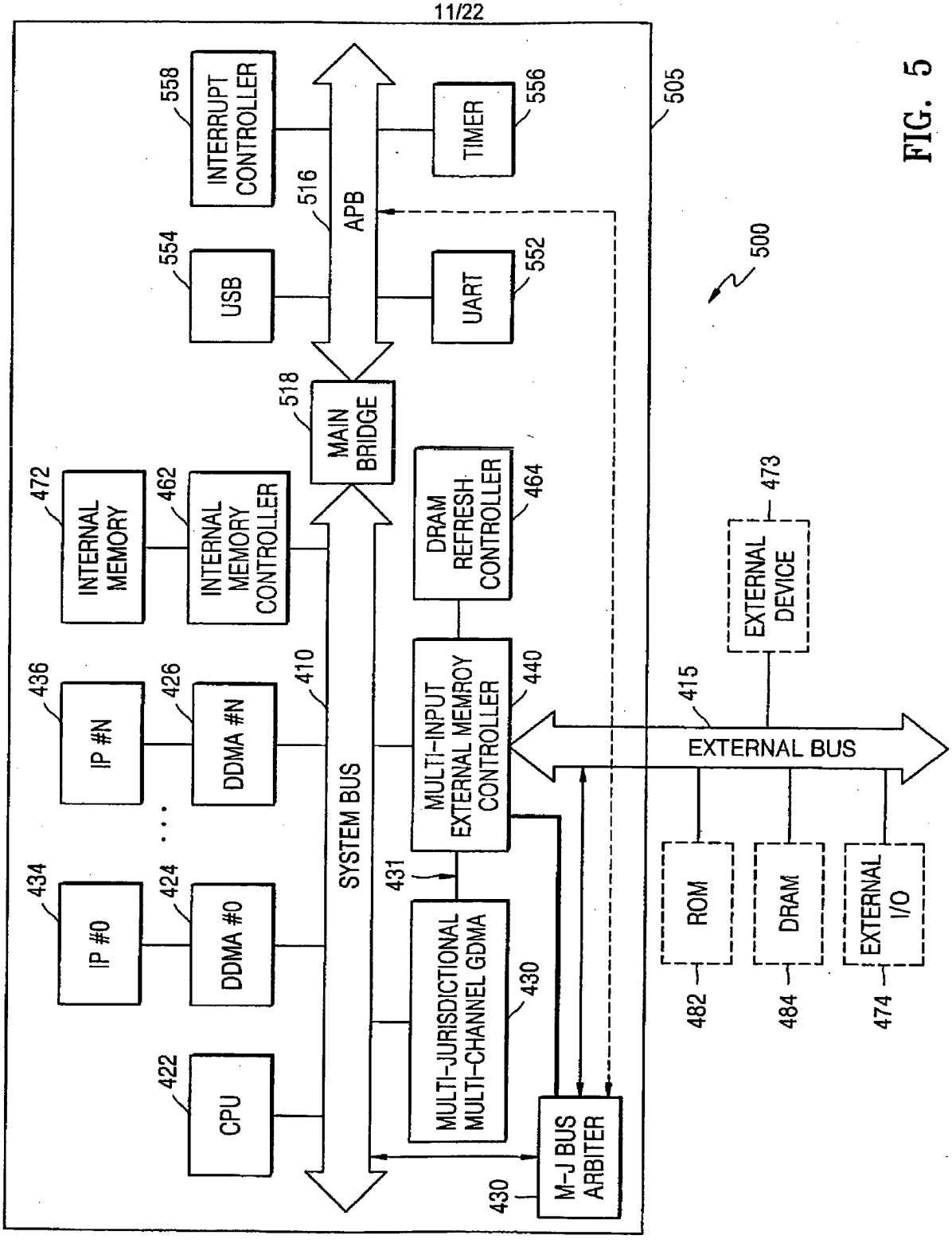

505
500
INTERRUPT CONTROLLER
558
TIMER
556
APB
516
USB
554
UART
552
MAIN BRIDGE
518
INTERNAL MEMORY
472
INTERNAL MEMORY CONTROLLER
462
DRAM REFRESH CONTROLLER
464
EXTERNAL DEVICE
473
IP #N
436
DDMA #N
426
410
SYSTEM BUS
MULTI-INPUT EXTERNAL MEMROY CONTROLLER
440
415
EXTERNAL BUS
IP #0
434
DDMA #0
424
431
MULTI-JURISDICTIONAL MULTI-CHANNEL GDMA
430
ROM
DRAM
EXTERNAL I/O
482
484
474
CPU
422
M-J BUS ARBITER
430

FIG. 5

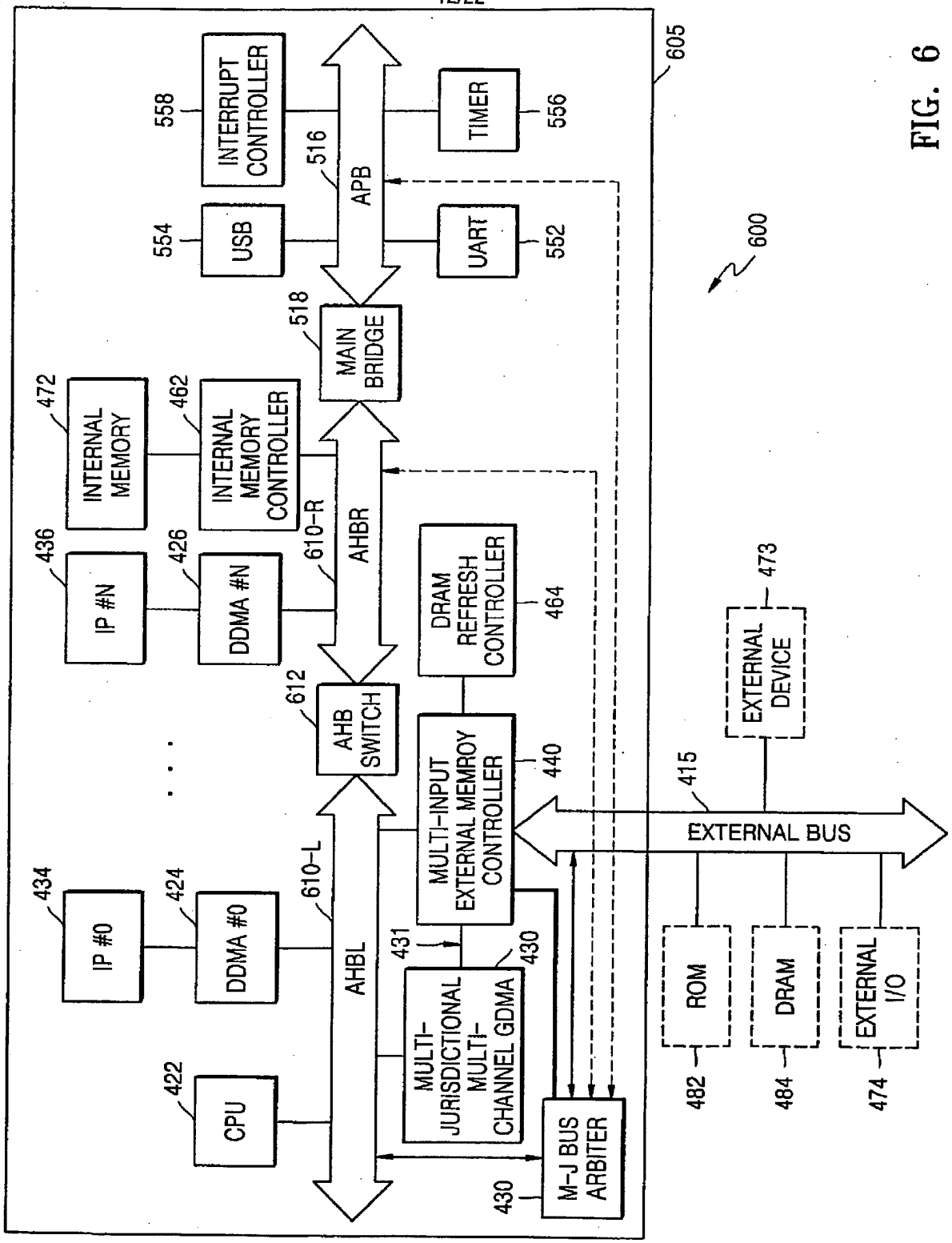
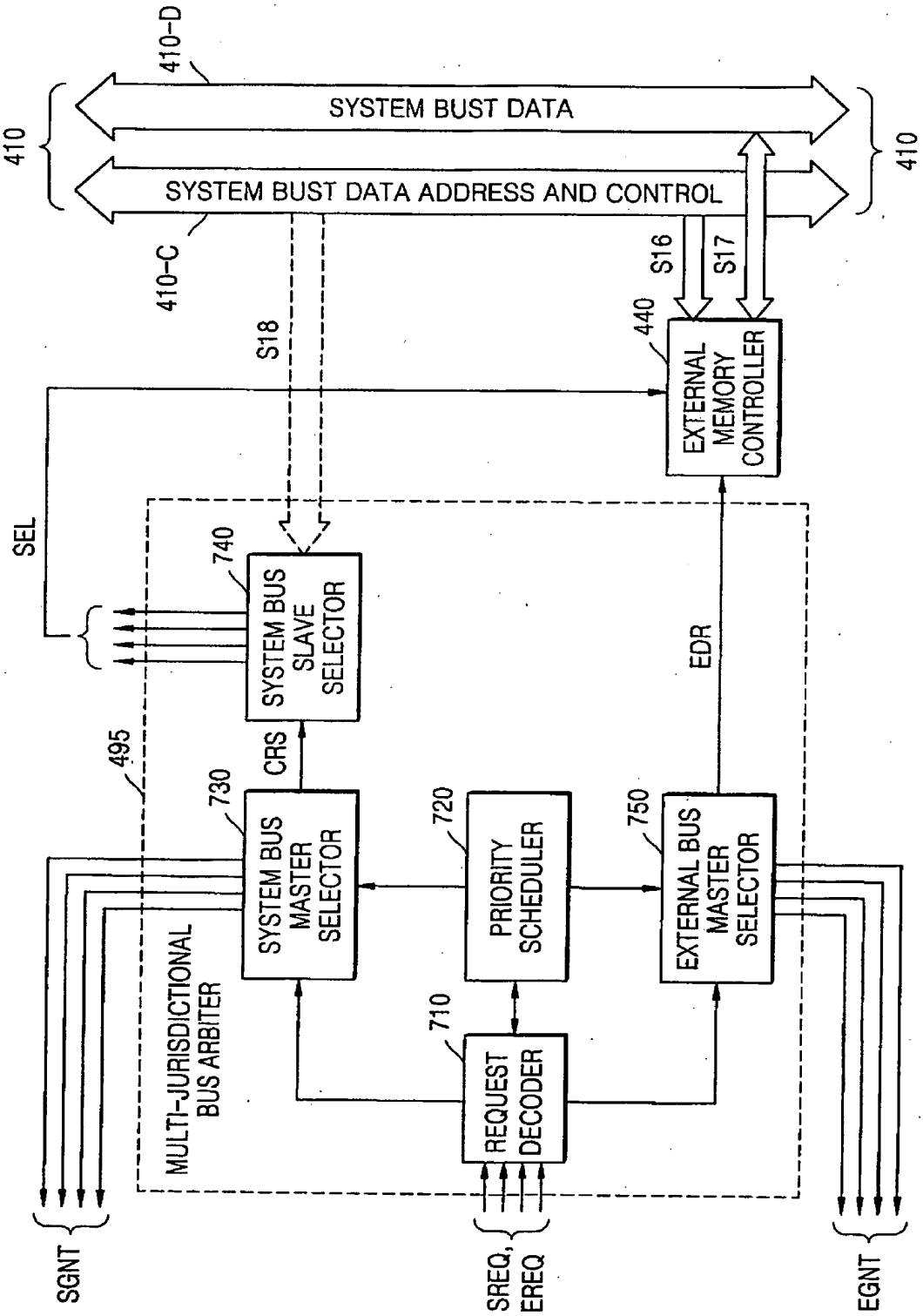


FIG. 6

FIG. 7



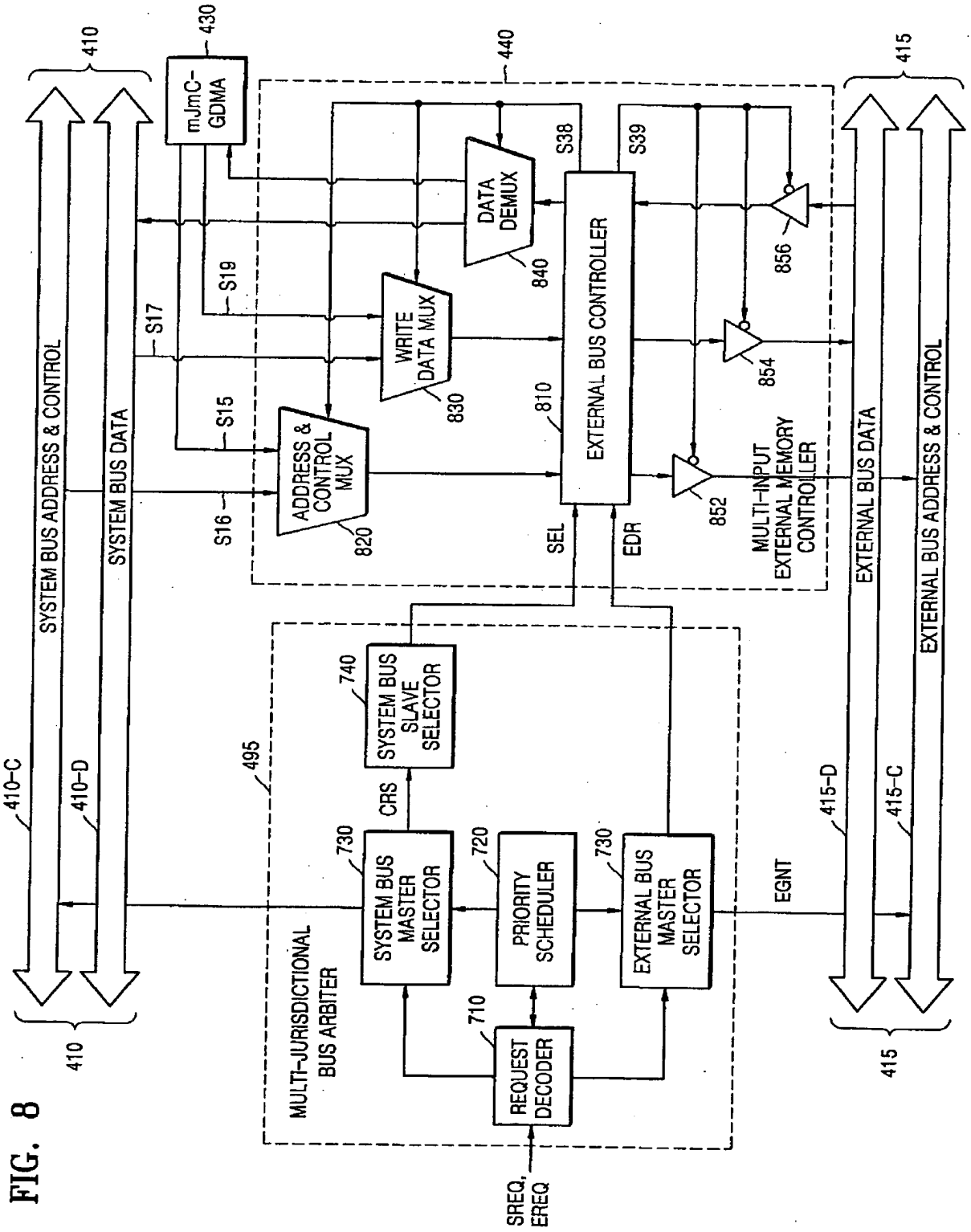


FIG. 8

FIG. 9

		EXTERNAL BUS MASTER	SYSTEM BUS MASTER	
	NO REQUEST REQ[1:0]=2' b00	EXTERNAL BUS ONLY REQ[1:0]=2' b10	SYSTEM BUS ONLY REQ[1:0]=2' b01	BOTH BUSES REQ[1:0]=2' b11
DRAM REFRESH CONTROLLER	O	O	X	X
CPU	O	X	O	O
DDMA BLOCK	O	X	O	O
GDMA CHANNEL	O	O	O	O
EXTERNAL DEVICE	O	O	X	X

FIG. 10

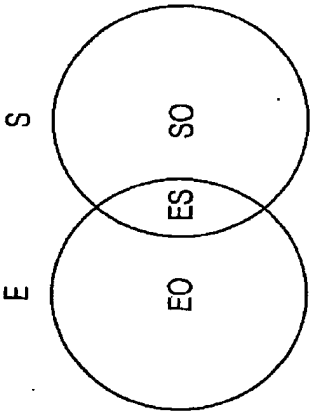


FIG. 11

CLASSIFICATION OF SET	ELEMENT
SET OF FUNCTIONAL BLOCKS MAKING A SYSTEM BUS REQUEST (SYSTEM BUS MASTER S)	CPU, DDMA BLOCK, AND GDMA BLOCK
SET OF FUNCTIONAL BLOCKS MAKING AN EXTERNAL BUS REQUEST (E)	DRAM REFRESH CONTROLLER, CPU, DDMA BLOCK, GDMA CHANNEL, AND EXTERNAL DEVICE
SET OF FUNCTIONAL BLOCKS MAKING ONLY A SYSTEM BUS REQUEST (SO)	CPU
SET OF FUNCTIONAL BLOCKS MAKING ONLY AN EXTERNAL BUS REQUEST (EO)	DRAM REFRESH CONTROLLER, GDMA CHANNEL, AND EXTERNAL DEVICE
SET OF FUNCTIONAL BLOCKS MAKING A REQUEST FOR BOTH SYSTEM BUS AND EXTERNAL BUS (ES)	CPU, DDMA BLOCK, AND GDMA CHANNEL
SET OF FUNCTIONAL BLOCKS MAKING REQUESTS FOR A SYSTEM BUS OR AN EXTERNAL BUS (A)	DRAM REFRESH CONTROLLER, CPU, DDMA BLOCK, GDMA CHANNEL, AND EXTERNAL DEVICE

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FIG. 12

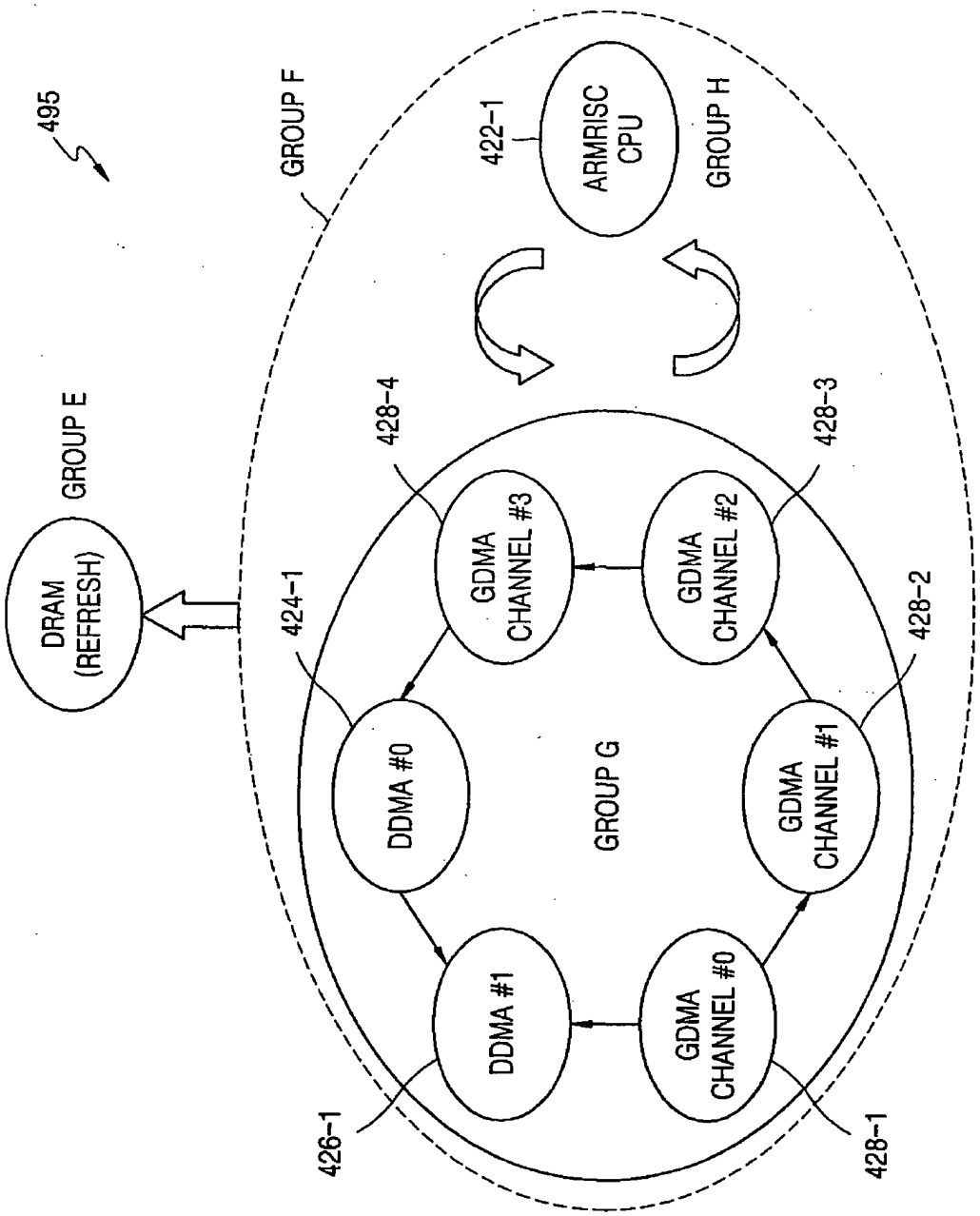


FIG. 13

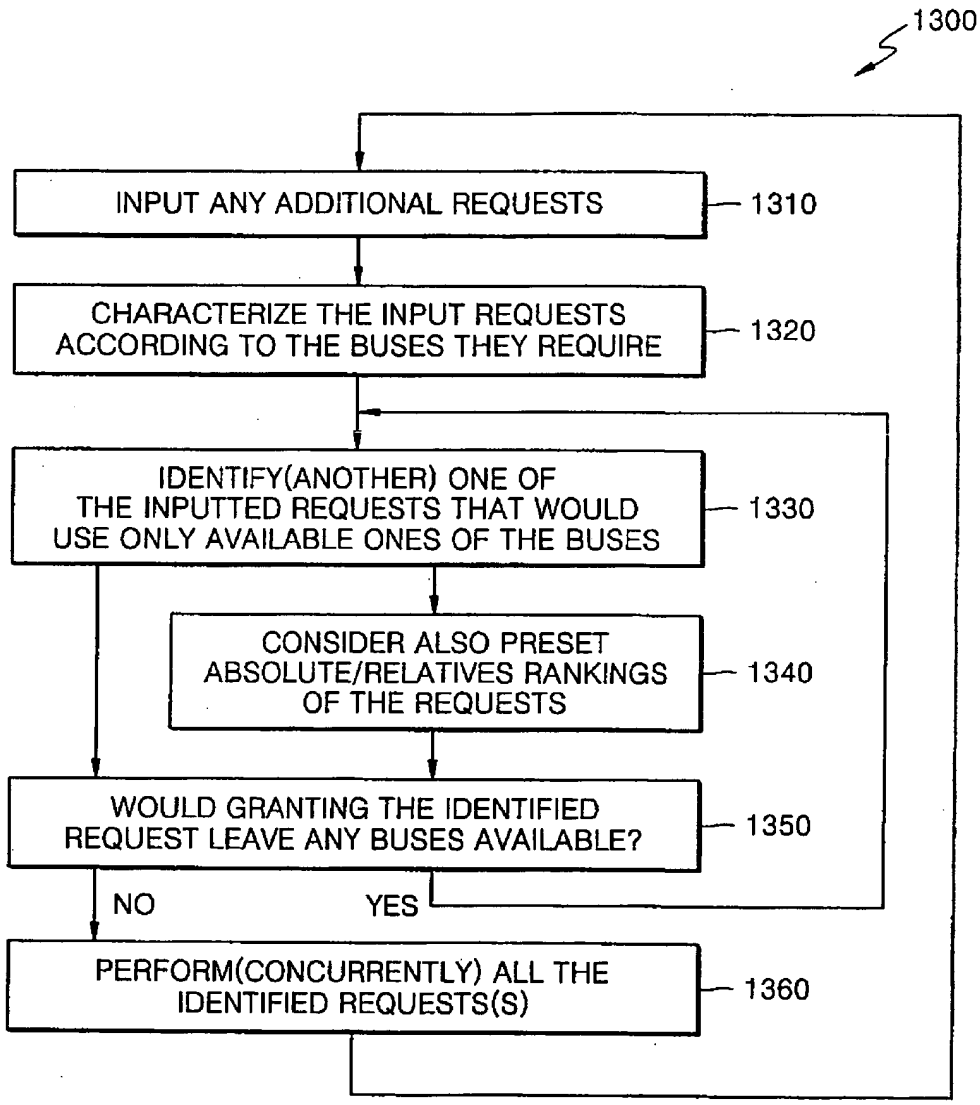

1300
INPUT ANY ADDITIONAL REQUESTS
1310
CHARACTERIZE THE INPUT REQUESTS ACCORDING TO THE BUSES THEY REQUIRE
1320
IDENTIFY(ANOTHER) ONE OF THE INPUTTED REQUESTS THAT WOULD USE ONLY AVAILABLE ONES OF THE BUSES
1330
CONSIDER ALSO PRESET ABSOLUTE/RELATIVES RANKINGS OF THE REQUESTS
1340
WOULD GRANTING THE IDENTIFIED REQUEST LEAVE ANY BUSES AVAILABLE?
1350
NO
YES
PERFORM(CONCURRENTLY) ALL THE IDENTIFIED REQUESTS(S)
1360

FIG. 14

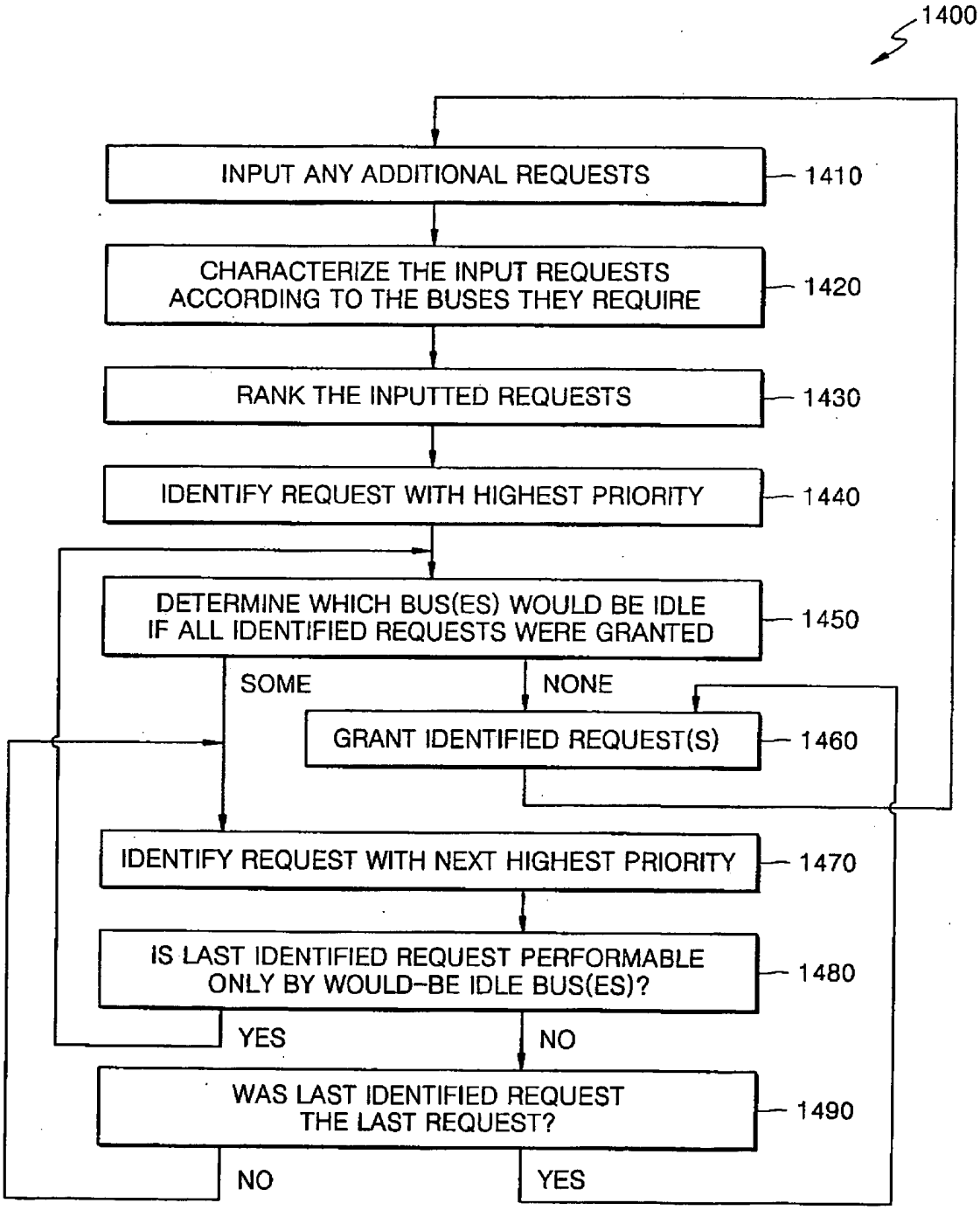
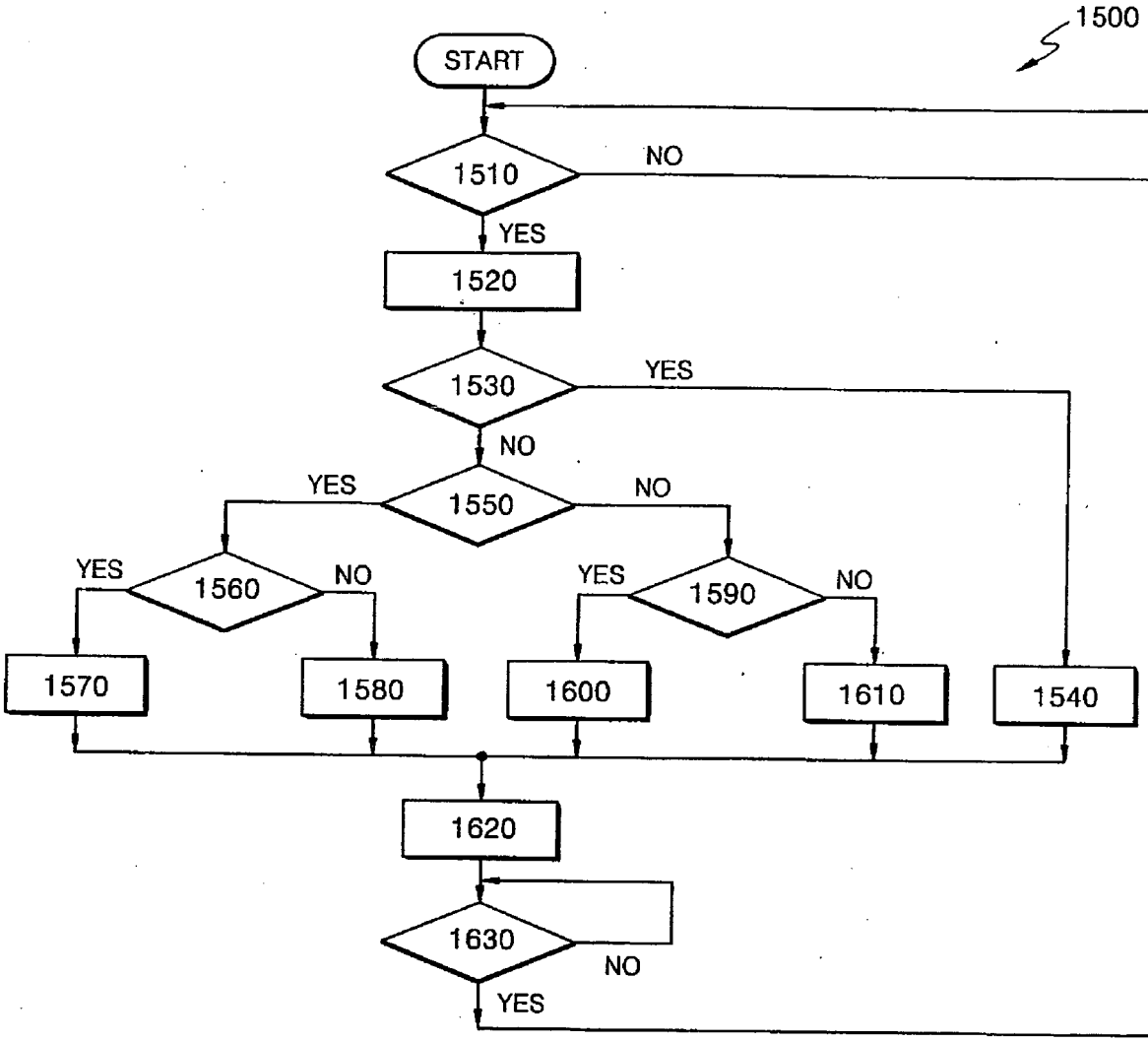


FIG. 15


1500
START
1510
NO
YES
1520
1530
YES
NO
YES
1550
NO
YES
1560
NO
YES
1590
NO
1570
1580
1600
1610
1540
1620
1630
NO
YES

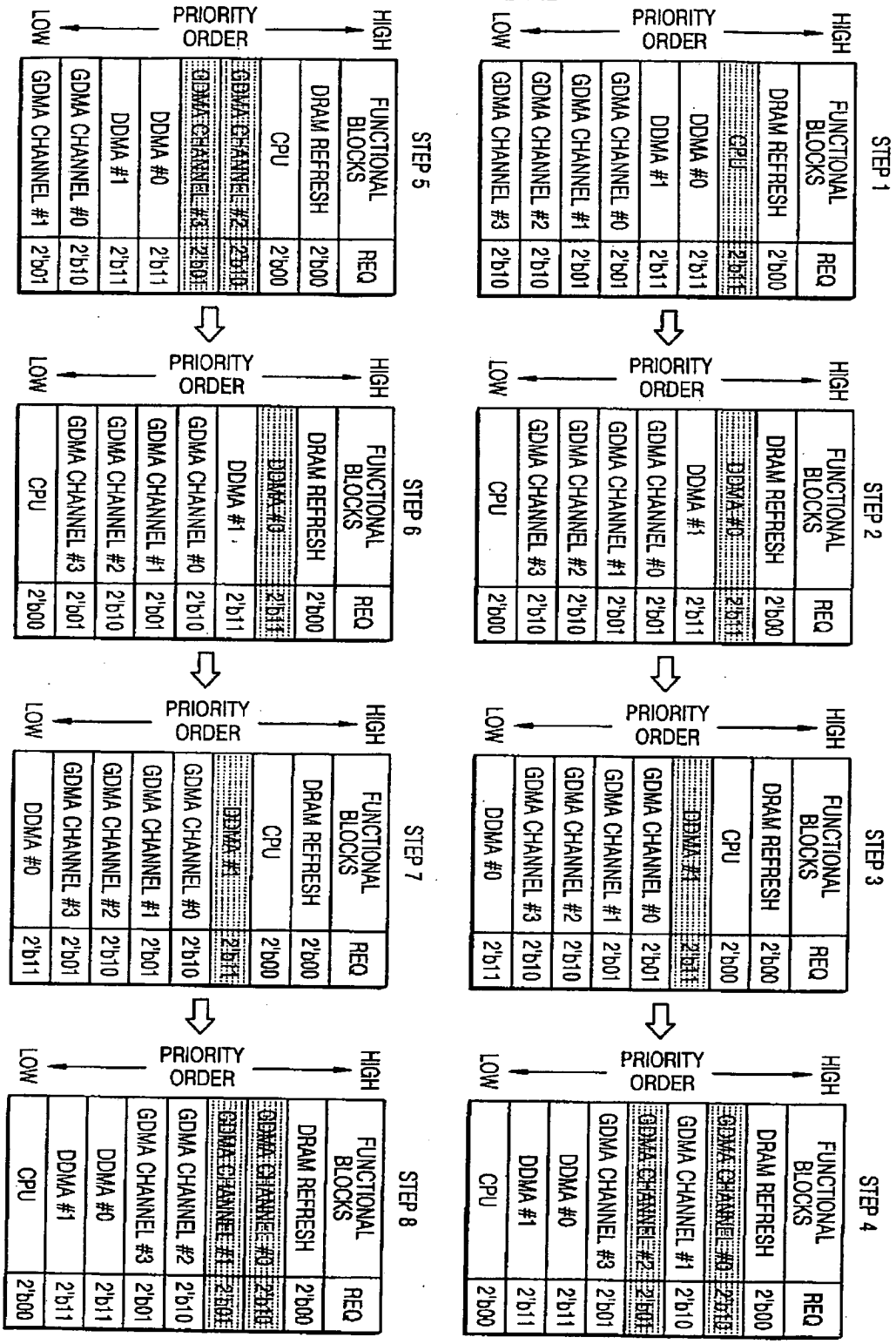

STEP 1
PRIORITY ORDER
LOW
HIGH
FUNCTIONAL BLOCKS
REQ
DRAM REFRESH 2'b00
DDMA #0 2'b11
DDMA #1 2'b11
GDMA CHANNEL #0 2'b01
GDMA CHANNEL #1 2'b01
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #3 2'b10
CPU 2'b00
STEP 2
DRAM REFRESH 2'b00
DDMA #1 2'b11
DDMA #0 2'b11
GDMA CHANNEL #0 2'b01
GDMA CHANNEL #1 2'b01
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #3 2'b10
CPU 2'b00
STEP 3
DRAM REFRESH 2'b00
CPU 2'b00
DDMA #1 2'b11
DDMA #0 2'b11
GDMA CHANNEL #0 2'b01
GDMA CHANNEL #1 2'b01
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #3 2'b10
STEP 4
DRAM REFRESH 2'b00
GDMA CHANNEL #1 2'b10
GDMA CHANNEL #0 2'b01
DDMA #0 2'b11
DDMA #1 2'b11
CPU 2'b00
STEP 5
DRAM REFRESH 2'b00
CPU 2'b00
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #1 2'b01
GDMA CHANNEL #0 2'b01
DDMA #0 2'b11
DDMA #1 2'b11
GDMA CHANNEL #3 2'b10
STEP 6
DRAM REFRESH 2'b00
DDMA #0 2'b11
DDMA #1 2'b11
GDMA CHANNEL #0 2'b10
GDMA CHANNEL #1 2'b01
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #3 2'b01
CPU 2'b00
STEP 7
DRAM REFRESH 2'b00
CPU 2'b00
DDMA #1 2'b11
DDMA #0 2'b11
GDMA CHANNEL #0 2'b10
GDMA CHANNEL #1 2'b01
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #3 2'b01
STEP 8
DRAM REFRESH 2'b00
GDMA CHANNEL #2 2'b10
GDMA CHANNEL #3 2'b01
DDMA #0 2'b11
DDMA #1 2'b11
CPU 2'b00

FIG. 16

FIG. 17

ITEM	PROBABILITY THAT ELEMENT HAVING BUS OWNERSHIP PERFORMS OPERATION			BUS UTILIZATION
	ELEMENT OF SET EO	ELEMENT OF SET ES	ELEMENT OF SET SO	
EXCLUSIVE BUS ARBITRATION	$\frac{1}{n(A)}$	$\frac{1}{n(A)}$	$\frac{1}{n(A)}$	$\frac{n(EO)+2n(EO)+n(SO)}{2n(A)}$
HIERACHICAL BUS ARBITRATION	$\frac{n(ES)+2n(SO)}{2n(S)n(EO)}$	$\frac{1}{2n(S)}$	$\frac{1}{n(A)}$	$\frac{4n(SO)+3n(ES)}{4n(S)}$
PRESENT INVENTION	$\frac{n(EO)+n(SO)}{n(A)n(EO)}$	$\frac{1}{n(A)}$	$\frac{n(EO)+n(SO)}{n(A)n(SO)}$	1